OPEN SOURCE SATELLITE

STM32H7 Radiation Test Report

VERSION 01
RELEASED

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1 Document History

Please see the following record of revisions:

Document Revision	Document Status	Change Description
01	RELEASED	Initial revision post internal review.

2 References

The following references are applicable to this document.

Document Reference	Document Title	Date	Reference in this Document
RM0433	Reference Manual: STM32H742, STM32H743/753 and STM32H750 Value line advanced Arm®-based 32-bit MCUs	Feb 2020	[STM32H7 Datatsheet]

3 Introduction

One of the key components of the Open Source Satellite (OSSAT) command and data handling system is the microprocessor for the On Board Computer (OBC). Microprocessors that have been designed to be radiation-hardened for the harsh space environment are expensive and tend to have poor performance compared to Commercial-Off-The-Shelf (COTS) equivalents that leverage the latest innovations in microprocessor technology. The OSSAT team possesses decades of experience in using COTS components in Low Earth Orbit (LEO) and intends to leverage the capabilities of the latest terrestrial technology in the development of the OSSAT platform computer.

The OSSAT team performed a research and development project to further the understanding of COTS processors, in partnership with the Surrey Space Centre (SSC) at the University of Surrey, UK, with support from Research England's SPRINT programme[1]. The OSSAT-SSC project team evaluated the latest available COTS microprocessors[2] and assessed their suitability in terms of performance with a view to test their resilience to the harsh space radiation environment. Three COTS processors were downselected and subjected to a series of research tests to determine processor performance and space environmental resilience.

4 Scope

This document is the second in a set of three reports that presents the results of the microprocessor research. Each document describes:

- The justified evaluation criteria for the selected processors.
- The key features of each processor.
- The results of the two types of tests performed on each processor:
    - A test of the processor's performance.
    - A test of the processor's susceptibility to the effects of the space radiation environment.

This second document gives the results of this research in relation to the second of the three downselected processors, the ST Microelectronics (ST) STM32H753.

5 Processor Selection

5.1 Selection Criteria

Several quantitative and qualitative criteria were defined in order to evaluate a suitable microprocessor to integrate into the OSSAT platform. This section presents the criteria with justifications listed in descending order of importance.

[1] https://sprint.ac.uk/about-us/

[2] https://www.sprint.ac.uk/news-stories/kispe-space-joins-sprint-to-source-microprocessors-for-next-generation-microsatellite-platforms/

5.1.1 Performance Requirement

The **minimum** performance figure of **200 DMIPS** has been defined.

5.1.1.1 Performance Requirement Rationale

The OSSAT team has experience in working with OBCs for a wide range of different missions. We are aware of the increasingly demanding performance requirements that flight software places on OBCs for new and emerging mission needs. For example: higher Attitude and Orbit Control System (AOCS) algorithm execution rates (in the range of 4-12Hz to support increased agility), higher telemetry sampling rates (in the range of 20Hz to improve the speed of anomaly diagnosis) and larger files (log data will be plaintext in order to reduce the time required to interpret the data).

Our survey of commercially-available space OBCs identified products that have a performance of 50 to 60 DMIPS, which do not satisfy the performance criteria required to enable a new generation of space-enabled missions, applications and services. The 200 DMIPS represents a substantial improvement in this performance without a significant increase in power consumption.

The availability of a very high-performance platform processor can lead to a blurring of the boundary between platform and payload because of the temptation to embed payload operations within such a processor, potentially leading to complicated and blurred functionality. Our design philosophy is to maintain a platform-payload separation to eliminate the risk of mission-specific payload requirements driving changes and NRE on the platform design.

NOTE: The DMIPS measure takes no account of floating-point operations.

NOTE: Manufacturers often measure performance in units of either Coremarks or DMIPS. We adopted DMIPS because it seemed the most common measure. Where manufacturers gave measurements in Coremarks, we translated the figures approximately into DMIPS.

5.1.2 Power Consumption Requirement

The maximum amount of power consumed by the processor must **not exceed 300mW** at ambient temperature.

5.1.2.1 Power Consumption Requirement Rationale

Power consumption is always a principal consideration on space missions. The platform must consume as little power as possible in order to maximise the power available for payloads and thereby enhance mission utility. The OSSAT team intends to capitalise on advances in low power processing technology to identify potential options that satisfy this requirement. It is also important to recognise that, when conducting a paper exercise, power consumption figures quoted by manufacturers can be difficult to interpret. A pragmatic and appropriate level of effort was applied to ensuring that the comparison of power figures is fair.

5.1.3 Floating Point Operations Requirement

The processor must be capable of processing arithmetic on **floating point numbers**.

5.1.3.1 Floating Point Requirement Rationale

The platform processor will need to perform AOCS algorithms at relatively high speeds (more than 4 Hz and up to 12Hz). To code these algorithms in integer maths is not practical. The processor therefore needs to support floating point operations. NOTE: this can be achieved either through the integration of a floating-point unit or otherwise through a compiler that can translate from floating point to integer maths through the compilation process. In this case, the general performance figure should be increased. As a preference, the processor would have a floating point unit (single or double precision).

5.1.4 Program Memory Requirement

The processor must be able to address at least **50MB** of **program memory** (the non-volatile memory used to hold the program).

5.1.4.1 Program Memory Requirement Rationale

Programs are anticipated to be in the region of 100's of kilobytes rather than 50MB. For example, KISPE recently integrated FreeRTOS with a Board Support Package (BSP) and a number of tasks all compiled down to <200kB of Program data on an ARM Cortex-M7. However, other Linux-based operating systems, that potential OSSAT users may wish to implement, have a much bigger footprint. Also, the introduction of run time uploadable tasks may result in far less efficient use of program memory. 50MB provides capacity to accommodate a wide range of programs. NOTE: This memory can be on-chip or off chip (with a preference for on chip so long as it has Error Correcting Code (ECC) protection).

5.1.5 Data Memory Requirement

The processor must be able to address at least **64MB** of **data memory** (the volatile memory used by the program during execution).

5.1.5.1 Data Memory Requirement Rationale

There are a number of consumers of data memory, including:

- Buffering data destined for the file system, depending upon file system performance, this may be significant.
- Buffer I/O.
- Data structures for the RTOS.

The OSSAT team have recently integrated FreeRTOS with a BSP and a number of tasks, all compiled down to use <400kB of data memory that was statically allocated). The amount of required memory may vary greatly and therefore 64MB was defined to address anticipated needs.

NOTE: This memory can be on-chip or off chip. Ideally, this memory would be on chip and with ECC protection.

5.1.6 Mass Memory Requirement

The processor must be able to accommodate at least **4GB** of **mass memory** to house the file system.

5.1.6.1 Mass Memory Requirement Rationale

Platform telemetry data will be stored alongside operational timetables that schedule activities and configuration files. This data will be stored in a file system that is housed on a mass memory. The mass memory should ideally be non-volatile so long as the file integrity can be maintained in environments susceptible to Single Event Upsets (SEUs). Some non-volatile memory needs to be baselined since the spacecraft configuration will be stored in a memory that needs to survive power interruptions and resets.

5.1.7 Thermal Requirement

The processor must be able to fully operate between -40 to +85 degrees C.

5.1.7.1 Thermal Requirement Rationale

This temperature range covers the majority of operating temperatures that will be experienced by the spacecraft. It is also the typical range for the majority of automotive electronic components that are being considered for OSSAT, giving the maximum flexibility to the thermal design of the spacecraft.

5.2 Qualitative Criteria

A number of other features and properties are relevant to the platform processor selection, including:

5.2.1 External Memory Interfaces

SEU memory protection can be implemented off-chip in hardware if the chip supports external memory interfaces.

5.2.2 Existing Radiation Tolerance data

Any existing data about the radiation tolerance of the processor would be beneficial. Furthermore, some parts have pin compatible radiation tolerant equivalents. These parts are potentially more relevant because the radiation tolerant equivalent part could be used for “beyond LEO” missions without needing to re-engineer these core elements of the platform software or PCB layout.

5.2.3 Existing SEU Protection

As the feature size of components has reduced, commercial processors have become susceptible to SEUs even when used in terrestrial applications. Therefore, some vendors have introduced error detection or error detection and correction technology into the silicon. Availability of SEU mitigation, such as single bit per word error detection and correction, is an important consideration.

5.2.4 Development Tool Compatibility

The availability of tools to aid the development of software for the processor and to model power consumption was considered, as was whether the tools are open source, whether support is available for a fee, and how large the userbase is.

5.2.5 RTOS availability

The quantity of Real Time Operating Systems (RTOS’s) that support the processor was assessed, as was whether the RTOS’s are open source.

5.2.6 Field-Programmable Gate Array (FPGA) configurability

FPGAs offer an extra degree of reconfigurability. FPGAs with embedded processors were therefore preferred and any FPGA hardware noted during the selection.

5.2.7 Cyclic Redundancy Check (CRC) Generation

Existence of hardware acceleration of CRC generation was evaluated because CRC generation will be a common task of the platform processor. It should be noted that the use of CRC protection should be weighed up against error detection and correction for communications interfaces.

5.2.8 Encryption/Decryption AES256

Existence of hardware acceleration to aid cipher/decipher was evaluated in order to satisfy the requirement for encryption to AES256: NOTE: the adoption of encryption must be weighed against power consumption, message sizes and the resulting effect on bit error rate.

5.2.9 Authentication (e.g. SHA-1)

Whether or not the processor includes hardware acceleration that aids authentication was assessed. This was considered because communications with the ground will need to be authenticated.

5.2.10 Flight Heritage

Previous in-orbit data, and information on the type of mission, if available, was evaluated.

5.2.11 Obsolescence

Production runs of components can be very short. This largely depends upon the industry for which the processor is manufactured. Chips manufactured for the automotive and aerospace industries are attractive because of the very long production runs, allowing the same components to be used across a series of different missions without needing to redesign the system.

5.2.12 Interfacing

The types and quantities of I/O interfaces that are supported by the chip was considered. Should specific technologies not be supported by the chip, supplementary devices could be used to provide the required interface.

5.3 STM32H7 Specification (Part #STM32H753ZI)

This is a very high-performance microcontroller with an ARM Cortex M7 core (see[STM32H7 Datatsheet]). It boasts 1027 DMIPS, consuming only 155mW during our test. This was one of the fastest processors we analysed for the platform computer that satisfied the criteria. It also has extensive ECC protection and fairly extensive memory interfacing. It hits all but the memory criteria.

The outcome of our analysis against the quantitative criteria is as follows:

Criteria	Target	Actual	Supplementary Circuitry required
Performance	200 DMIPS	1027 DMIPS[3]	N/A
Power Consumption	300mW	155mW during radiation test	N/A
Floating Point	FPU desirable	Single & Double Precision FPU	N/A
Program Memory	50MB	2MB (internal)	External program memory
Data Memory	64MB	1MB (internal)	External data memory
Mass Memory	64GB	None (other than the data memory already mentioned)	The External Bus Interface can map up to 1GB of external memory (parallel memory e.g. SRAM). It can also support serial memories too. NOTE: SD/MMC memory can be to interface but gives very high memory densities. This presents a risk (small transistor sizes could result in many SEUs and the memory could be slow to access).
Thermal	-40 to +85 degrees C	-40 to +85 degrees C	N/A

The outcome of the chip against the qualitative criteria is as follows:

Criteria	SAMV71 capability
External memory interfaces	There are an extensive number of external memory interfaces (both parallel and serial).
Existing radiation tolerance data	None found.
Existing SEU protection	ECC protection in the cache (see Appendix A), the tightly coupled memory, the internal SRAM and 8k of the external Flash (but not other external memory interfaces). The tightly coupled memory and internal SRAM are protected to single-error correction and double error detection.

[3] This assumes the cache memory (which is ECC protected) is enabled.

Criteria	SAMV71 capability
	The internal Flash memory has ECC protection (1 bit error correction and 2 bits error detection per 256 bits word. The external NAND Flash interface has ECC protection for up to 8k of memory, capable of correcting a single bit and detecting 2 bit errors per 256, 512, 1024, 2048, 8192 read/write operation.
Development tools	STMCube is a free and quick start tool that generates source code. Also, FreeRTOS ports exist, GNU toolchain is also available. The tools are used widely (because the chips are used widely). The tools from ST do not have supported except through online forums. There appears to be a power consumption calculator as part of STMCube that accounts for the peripherals that are in use.
RTOS availability	The Open Source FreeRTOS is a popular, open source choice for this and other ARM based microprocessors. Existing compatible BSPs exist for a great many RTOSs.
FPGA configurability	This chip is not included within an FPGA; however an external FPGA could be incorporated in the platform computer design.
CRC Generation	A generic CRC generation hardware acceleration is included. This means that CRCs generated for example,. CCSDS comms can be generated in hardware.
Encryption/Decryption	Hardware Acceleration for: DES/TDES 64-128-192 AES: 128,192,256
Authentication	Hardware Acceleration for: SHA1/256
Flight Heritage	None: this is a relatively new chip although STM32 family chips are baselined on many European missions.
Obsolescence	This is a popular part with a likely long production run, it is designed for the automotive industry.
Interfaces	4 * I2C 8 * UARTS 6 * SPI 2 * SD/MMC 2 * CAN FD (1 with TT-CAN) 36 * ADC channels 2 * 32-bit timers 10 * 16-bit timers

5.4 Evaluation Summary

The STM32H7 matches the defined evaluation criteria well from the perspective of power consumption, run-time processor power and floating point support but lacks the required memory. Therefore, it would need some supplementary external memory.

6 STM32H7 test results

Following the down-selection of this chip, the following tests were performed using evaluation hardware.

6.1 Total Ionising Dose Radiation Test

6.1.1 Test Setup

6.1.1.1 Test Facility

The Realistic Electron Environment Facility (REEF), located at the University of Surrey, UK, and operated by research colleagues from SSC exposes samples in vacuum to a ~2.5 GBq Sr-90 source. Strontium-90 provides an excellent practical option for the provision of long-duration, low-intensity exposures as it allows uninterrupted irradiations over the required long periods with an electron spectrum that is appropriately representative of the real space environment.

Figure 1: REEF equipment at the University of Surrey

The REEF can be used to test materials and components for their vulnerability to both internal charging and total ionising dose phenomena. The dose rate is proportional to electron current and thus is primarily determined by the source-to-sample separation distance in the experimental setup. Changes to the electron spectrum change due to component shielding. This was taken into account (see section 6.1.4.1).

The dynamic range of normal incident electron current achievable with REEF is wide, ranging from ~6 pA/cm^2 at low (~3.5 cm) source-sample separation to ~0.3 pA/cm^2 at high source-sample separation (~16 cm). Higher currents can in theory be achieved at even smaller separations, though this would be at the expense of the assumption of normal incidence irradiation. Further reductions in current are achieved by adding planar aluminium shielding in between the source and sample.

The processor components to undergo testing were exposed to radiation equivalent to a 10 year, 800km, sun synchronous LEO mission. Upon completion of the REEF test for each board, any boards that showed forms of damage were tested again outside REEF to test for any potential annealing effects following irradiation.

6.1.2 The Target Under Test

In order to generate statistically relevant information, four STM32H7 Eval2 evaluation boards featuring the downselected chip (the “Target”) were irradiated.

Figure 2: STM32H753XI-EVAL2 Eval Board: Image Credit: ST Micro
NOTE: This image from the user guide includes the LCD screen, which needs to be removed prior to testing.

The intent of the test was to assess the radiation tolerance of the processor only, therefore the LCD screen was removed and rest of the components were shielded from the radiation source.

Each evaluation board was placed inside REEF and the radiation source positioned in order to test at a 1 kRad/hr dose rate as shown in Figure 3.

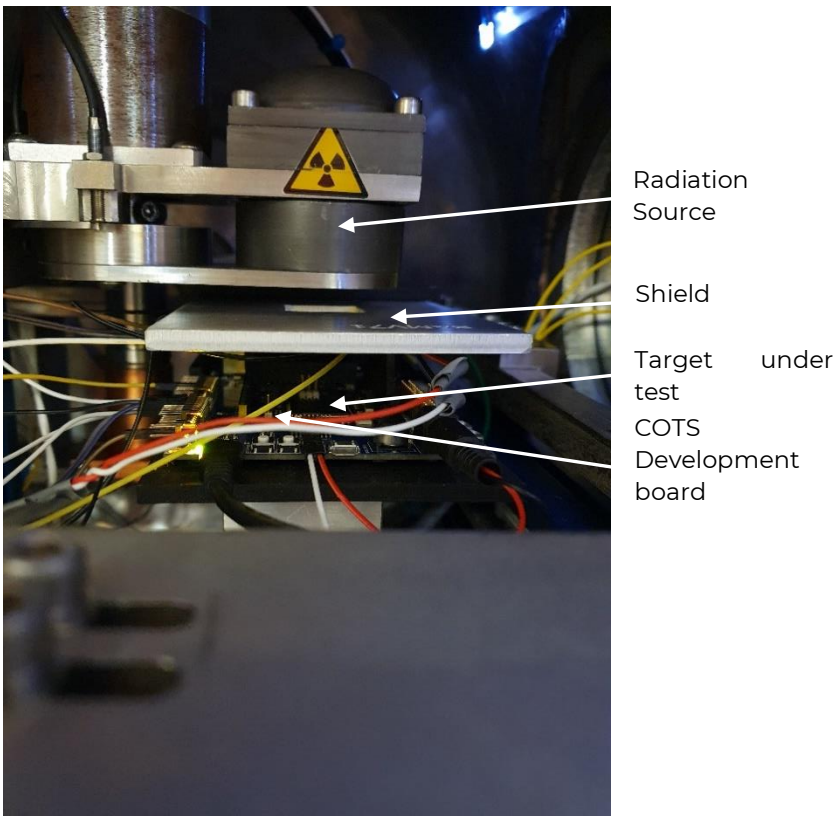

Figure 3: SAMV71 inside REEF

6.1.2.1 Target Software

The target processor was powered during irradiation. It ran software exercising various I/O interfaces and memories. The Test cycle repeated autonomously as illustrated in Figure 4 (NOTE: the wait between tests was reduced to 3 seconds in contrast to this figure. The original rationale for 30 seconds related to the anticipated time required to ensure a current & voltage measurement during the test. However, the current and voltage measurement mechanism proved faster than anticipated).

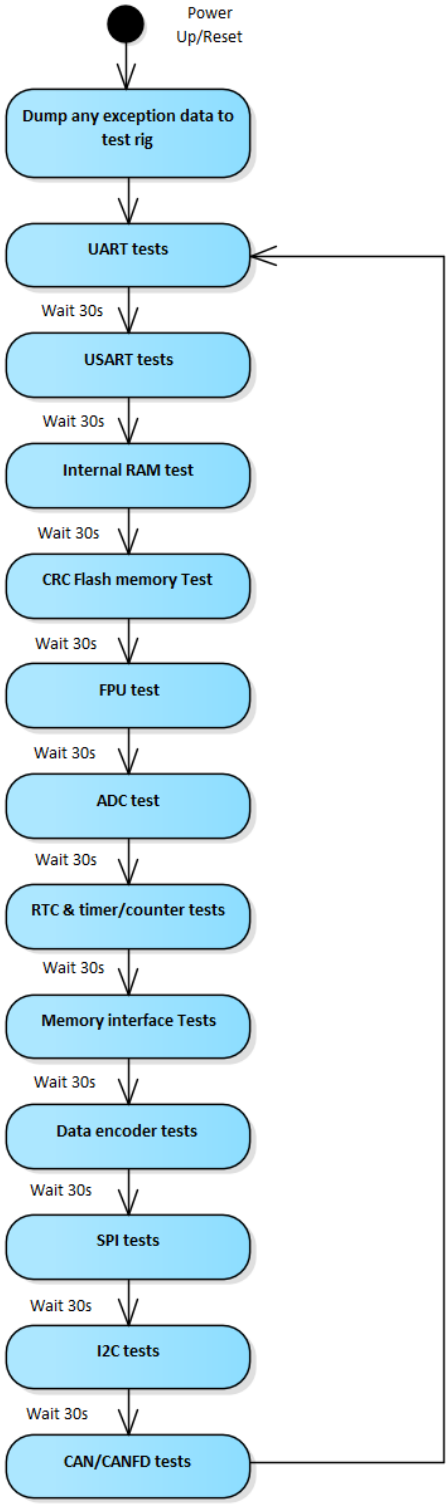

Figure 4: SAMV71 in test software loop

The tests were as follows:

- The I/O test for UART and USART test included signalling at the physical layer which were looped back so that both transmission and reception were tested.
- The on chip RAM was tested using a scrub, read, write method.

- The internal Flash memory executed the code to perform all of these tests, a CRC of the Flash image was stored to an SD card and the Flash memory CRC was calculated once per test loop and compared to the value in the SD card.
- The Floating Point Unit was exercised using a ray tracing algorithm.
- ARM exception handlers were written to output the value of the exception registers should exceptions occur during code execution.
- NOTE: Time did not allow for the development of software to support the testing of the Real Time Clock, the timers, counters, AES encoder/decoder, ADC, I2C, SPI and ECC. Tests were limited to those that were considered essential.

All of the above tests and exception handlers output data were sent across both a CAN bus and a UART to a test PC that collated the information.

6.1.3 Test Rig Setup

The test rig setup is illustrated as shown below.

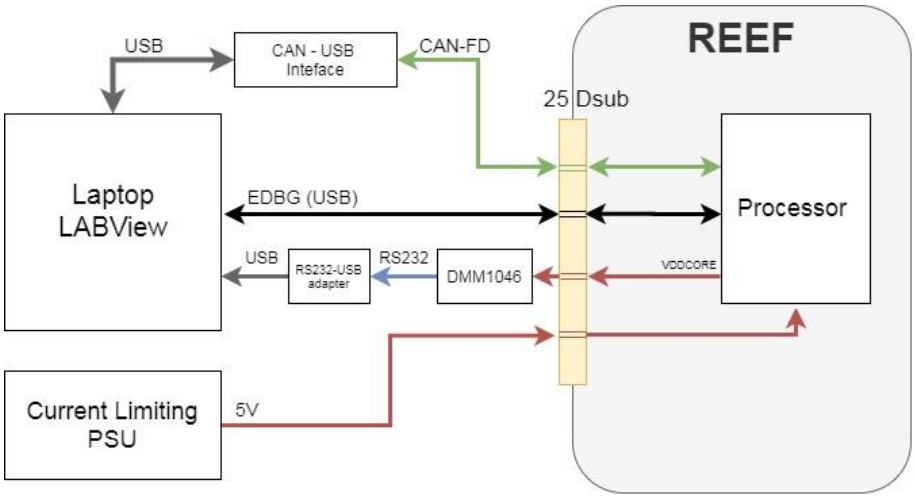

Figure 5: REEF Test rig setup

Test data was transmitted via two channels:

- A UART that the STM32H7 Eval2 multiplexes into a USB channel using ST's ST-Link protocol (labelled EDGB above).
- A Controller Area Network (CAN bus).

Two dissimilar communications channels were chosen in order to mitigate the possibility that the radiation dose affected one of these channels but not the rest of the chip under test. A test was also conducted of the CAN bus integrity (to ensure that the STM32H7 CAN controller was functioning correctly). This CAN test involved both transmission and reception of CAN data to and from the target.

Alongside the above tests, the current and voltage to the chip under test was monitored using a Digital Multi Meter (DMM).

All of the above data was captured to a comma separated text file alongside the current radiation dose using a LABView program that interfaced to the DMMs, the

CAN bus and the UART (through EDGB). The LABView program also incorporated a Graphical User Interface (GUI) that gave real time feedback to an operator. The GUI is shown below.

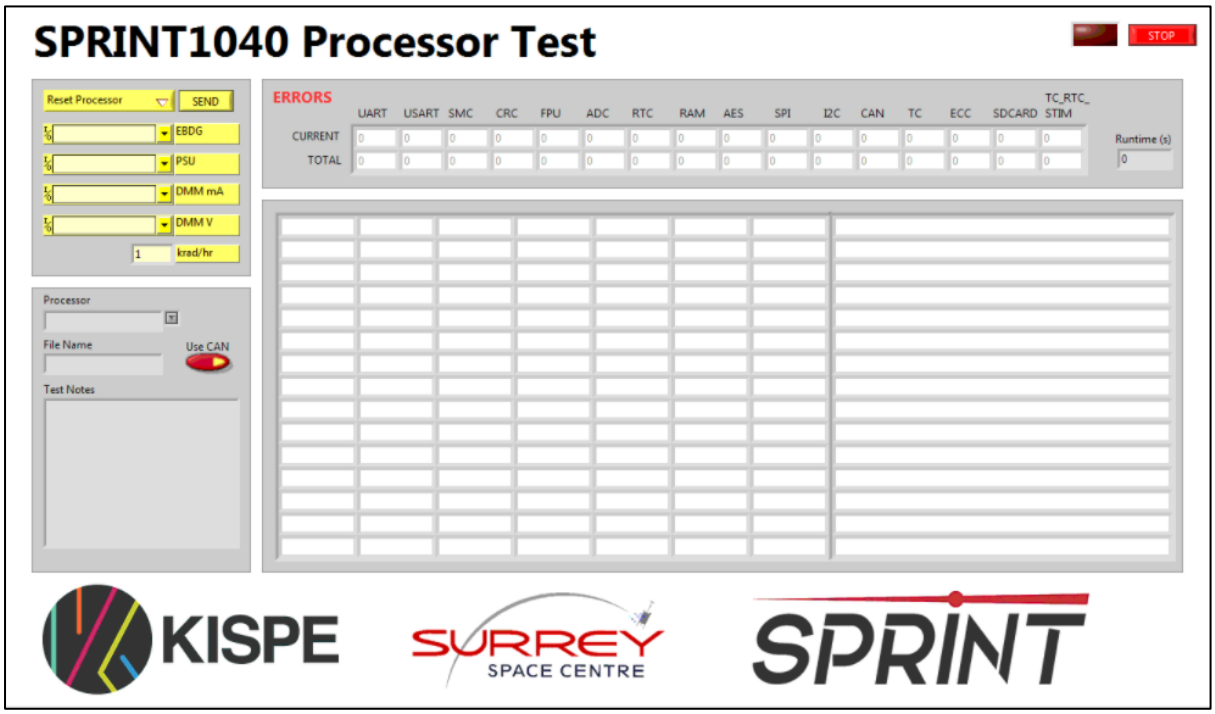

Figure 6: REEF Test Rig Utility GUI.

Testing was automated such that the system automatically attempted to resolve errors by resetting the peripheral causing the error using a stepped approach such as illustrated for the I/O tests in Figure 7. This involved a combination of functions on the target (highlighted blue) and functions of the test rig utility (highlighted red). The number of failures were held in a non-volatile memory (SD card) such that the progression through the failures was maintained by the target through power cycles of the target.

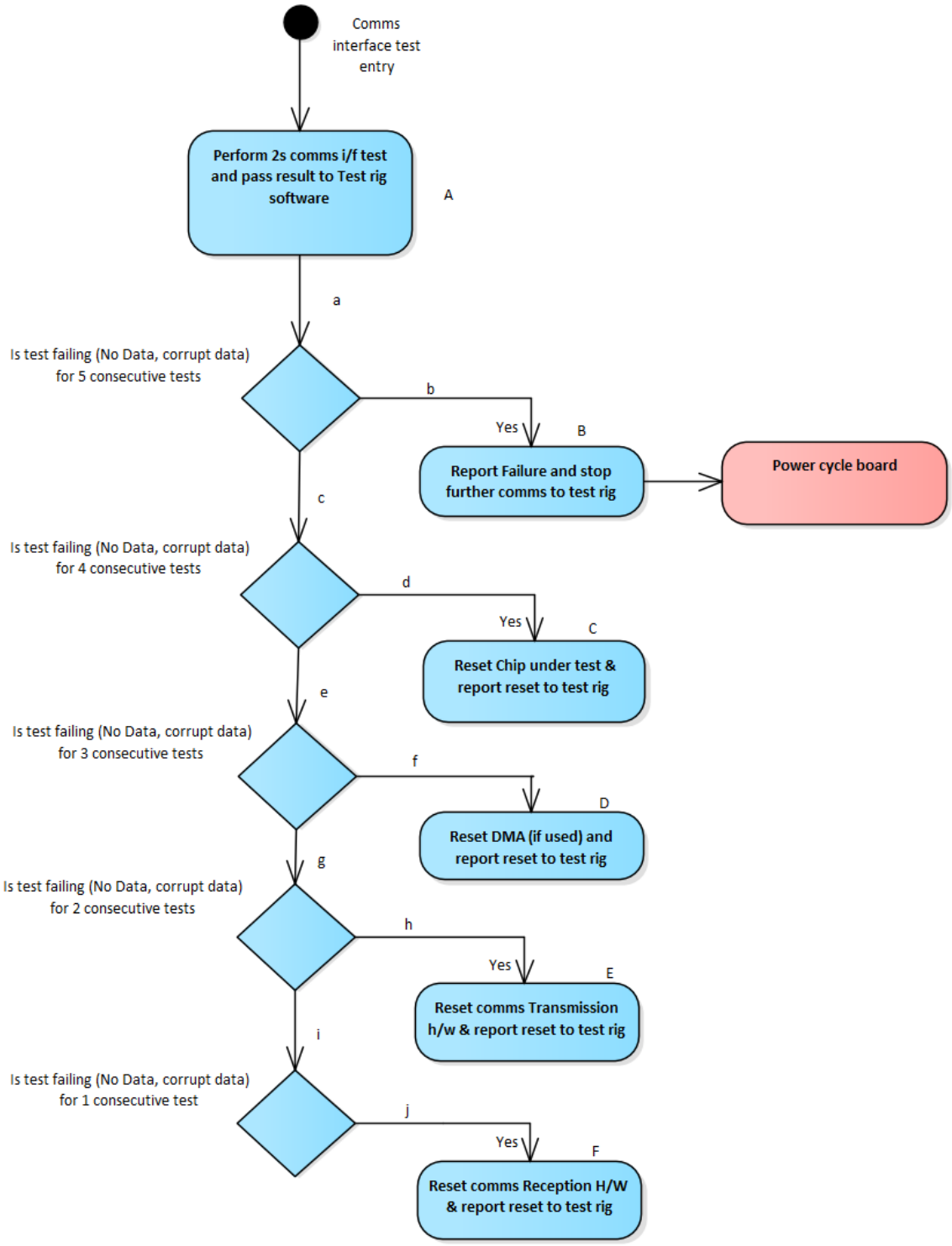

Figure 7: Automatic recovery from I/O interface errors

This mechanism allowed the tests to be conducted without operator interaction which allow the tests to run whilst being compliant with COVID-19 restrictions applied by the University of Surrey during 2020 and 2021.

6.1.4 Test Analysis

This section summarises the radiation environment calculations used to plan the experimental work for test board irradiations in REEF. The expected total ionising dose (TID) over the course of a nominal mission, and the dose rate within the test facility at the University of Surrey were calculated.

6.1.4.1 ORBIT ANALYSIS

The Space Environment Information System (SPENVIS) was used for both the radiation environment specification (trapped protons, trapped electrons and solar protons) and the dose-depth calculations. The following inputs were used:

- 800 km sun synchronous orbit
- 10 year mission duration
- Standard trapped environment models AE8 and AP8
- SAPPHIRE solar proton model (at 90% confidence over 10 year mission duration)
- SHIELDOSE-2 used for dose-depth with planar shielding geometry
- Spacecraft shielding assumed to be 2mm

Trapped proton and electron fluxes in the Van Allen belts were calculated via SPENIVS using the standard AE8 and AP8 environment models. Figure 8 shows example integral flux maps above 2 MeV and 10 MeV for electrons and protons respectively.

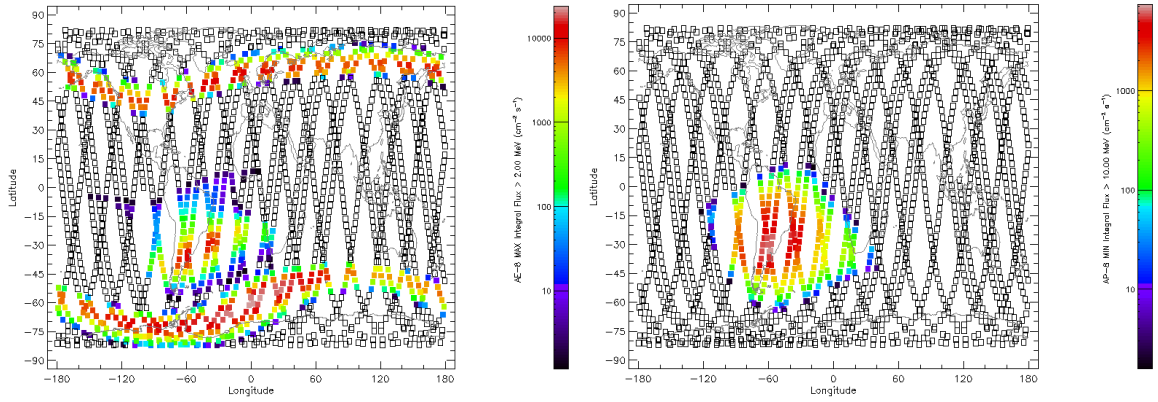

Figure 8: Integral flux maps for >2 MeV electrons (LHS) and >10 MeV protons (RHS) overlaid on a 800 km sun synchronous orbit trajectory.

Differential spectra from these calculations are shown in Figure 9. Also shown is a spectrum for solar energetic protons (SEPs) over the 10-year mission duration. As SEP occurrence is a probabilistic process, this spectrum is shown at the 90% confidence level (i.e. there is a 90% probability that the fluence will not be exceeded over this time frame).

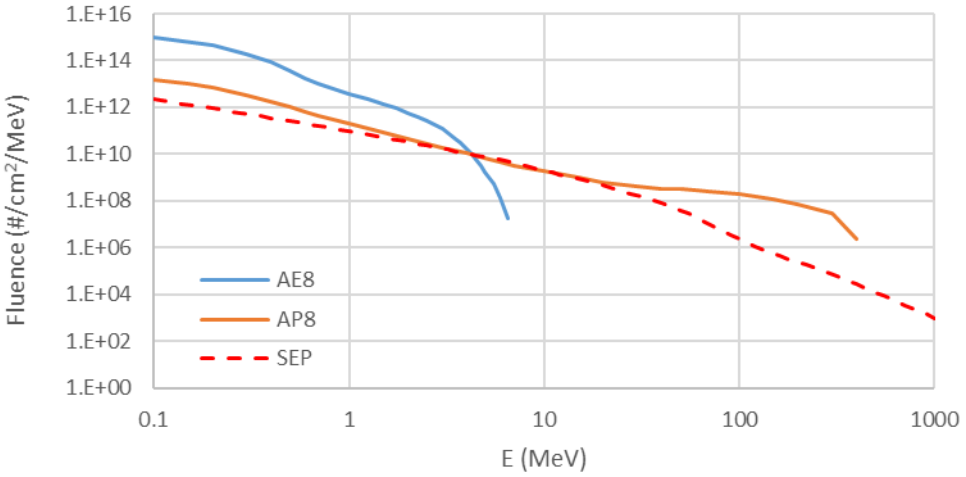

Figure 9: Differential electron and proton spectra for a 10 year period in 800 km sun synchronous orbit. Trapped spectra are shown for electron (AE8) and protons (AP8) and cumulative solar protons (SEP) calculated using the SAPPHIRE model are shown at the 90% confidence level.

Ionising dose as a function of shielding depth was calculated with SHIELDOSE-2 using the spectra shown in Figure 10. Planar shielding geometry was assumed as this is most suitable for locations that are relatively lightly shielded (at higher levels of shielding spherical geometry is more appropriate). It is clear from this plot that the influence of solar protons on dose is likely to be negligible for this environment – this is useful as it allows linear scaling of dose values for different mission durations.

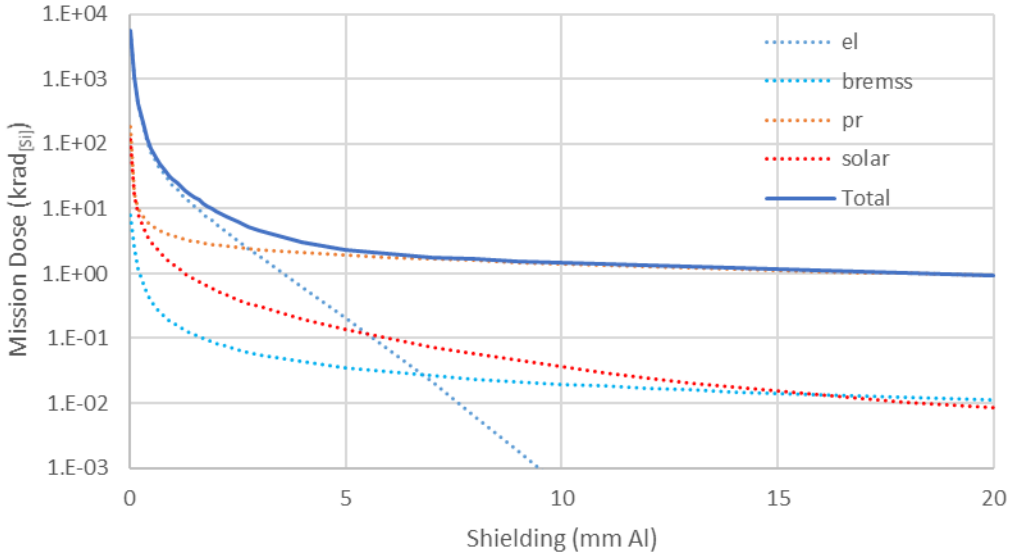

Figure 10: Ionising dose as a function of shielding depth (aluminium-equivalent) over the course of a 10 year LEO mission. A planar (slab) geometry is assumed. Contributing components ("el" = electron direct ionisation, "pr" = proton direct ionisation, "bremss" = Bremsstrahlung radiation and "solar" = SEPs at 90% confidence) are shown as dotted lines.

For example, these calculations predict a total ionising dose of ~3 $kRad_{[Si]}$ over the 10 year LEO mission if 4 mm Al-equivalent shielding were assumed. The figure for 1 mm of Al-equivalent shielding is an order of magnitude higher at ~30 $kRad_{[Si]}$, and the figure for 2mm of shielding is 9 $kRad_{[Si]}$. The assumed level of spacecraft shielding is critical in determining the appropriate dose to evaluate the performance of candidate components.

6.1.4.1.1 REEF Calculations

Monte Carlo particle transport calculations were used to simulate a simple planar geometry whereby a 100 micron silicon sensitive volume is shielded by a 100 micron layer of fused silica (SiO_2) packaging material. The source itself is encapsulated with a thin layer of stainless steel attenuating the raw strontium-90 beta spectrum before incidence on the device under test. Figure 11 shows the raw and attenuated spectra alongside the additional (albeit small) attenuation due to component packaging. The estimated dose rate for an incident current of 1 pA/cm^2 (corresponding to a source-sample separation of approximately 9 cm) is ~1 $kRad_{[Si]}$ per hour. This dose rate could potentially be increased substantially by reducing the source-to-sample separation, however, as the strontium is (approximately) a point source, too high a dose rate could potentially introduce uncertainty due to anisotropy of the irradiation. It has been calculated that the micron layer thickness of the processor packages only makes a minor difference to the total TID and should be considered a minor risk.

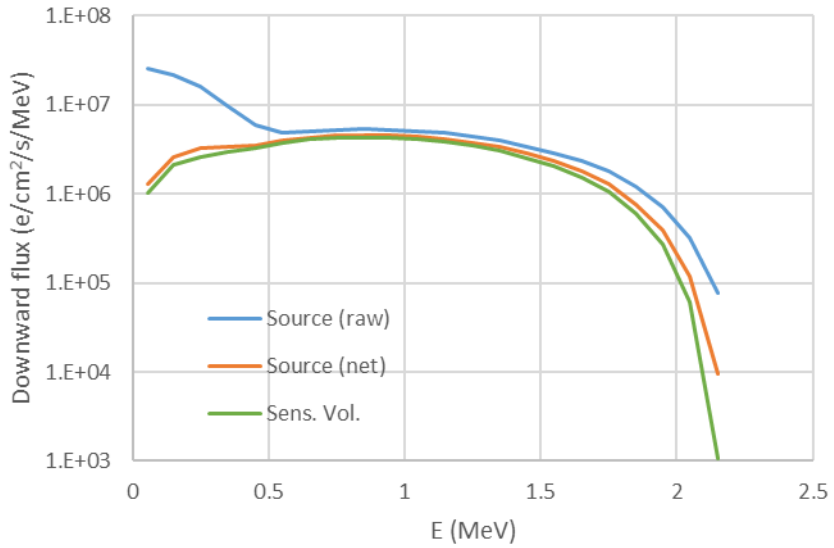

Figure 11: REEF electron spectra for the raw source (blue line), net source spectrum after encapsulation packing (orange line) and spectrum after nominal component shielding (green line). Although the impact of source encapsulation on the spectrum is clear, the impact of thin layers of component shielding is relatively small.

6.1.4.1.2 Summary

Standard radiation environment tools were used to calculate the total ionising dose for a 10 year mission in 800 km LEO. The dose has a strong dependency on assumed spacecraft shielding, for example ranging from ~3 $kRad_{[Si]}$ to ~30 $kRad_{[Si]}$ for 4 mm and 1 mm Al-equivalent shielding respectively. In parallel the dose rate in REEF at a particular reference point for incident electron current (~1 $kRad_{[Si]}$ per hour) was calculated Therefore, based upon the specification of 2mm shielding, the expected dose will be ~9 $kRad_{[Si]}$. The conclusion was that the total mission dose could be achieved in REEF in a timescale of hours to tens of hours of exposure. Significantly higher and lower dose rates are achievable; however these are unlikely to be necessary unless it is desirable to expose devices under test to doses far in excess of the expected mission dose.

6.1.5 Test Plan

Given the above test analysis, the team decided to test four targets to 10 kRad. This was considered the pass criteria for a 10 year, 800 km sun synchronous mission. Should time allow and the target survives this dose, the plan was to expose one of these four parts to as high a dose as was achievable before observing failures through the test rig utility.

6.2 STM32H7 Results

6.2.1 Overview

Boards Tested: 4/4

Batch Markings:

A. 7BA5B, 28 VQ V, PHL, 7B 9 13

Board	Batch	Test Time (hrs)	TID (krad)	Start Voltage (V)	End Voltage (V)	Start Current (mA)	End Current (mA)	NOTES
1	A	16.6	25 & 29 (see NOTES)	3.313	3.313	37.86	38.98	1.5 krad/hr dose rate Testrig OS crashed at 3.9 krads when running overnight. Testrig was restarted at 25krads and all tests passed up until 29krads where the test was stopped
2	A	18	27	3.32	3.32	39.35	40.44	1.5 krad/hr dose rate SD_CARD error at 22.8 krads. This caused SD CRC value to be set to 0, causing subsequent CRC errors for remainder of the test. NOTE: KISPE do not plan to make use of an SD card in orbit.
3	A	6.5	10	3.299	3.299	39.39	40.04	1.5 krad/hr dose rate No Failures
4	A	66.6	100	3.29	3.29	38.06	46.59	*Destruction Test* 1.5 krad/hr dose rate

								At 47 kRads, processor exceptions when observed during the CRC integrity test of the Flash memory. It is likely that the internal Flash Memory began to fail at 47 krads. Initialisation process failing at 98 krads. Power cycles failed to restart the processor correctly. Often 5-10 power cycles were required before comms received again.

6.2.2 Evidence Files

Board 1: STM_BOARD1_REEF.txt + STM_BD1_POST 25k. txt

Board 2: STM_BOARD_2_REEF.txt

Board 3: STM_Brd3_REEF.txt

Board 4: STM_DESTRUCTION.txt

These raw data files are available by request to the OSSAT team. We are happy to supply this information but it needs to be supplemented with a format description.

6.2.3 Error Recovery Actioned

Board	Error Recovery Steps Actioned	Results
1	None	N/A
2	SD_CARD Interfaced Memory	All CRC error recovery steps actioned. Power cycles did not solve the error, as the CRC read value stored on the SD card had been reset to 0.
3	None	N/A
4	Flash memory CRC: The Test rig Power Cycled the target in order to recover from the failure of the flash memory integrity check.	Power cycling the target resulted in successful recoveries. However, the recovery action from these failures became less effective with increased dose and at 97 kRads the processor was not always recovering through a power cycle.

6.2.4 Observed Failures/Recoveries

6.2.4.1 SD_CARD Reset

During the test run of Board 2, there was an unexpected error during a test of the SD card, that was not correctly reported to the test rig. This error was not repeated during the remainder of the test. This can be seen in the following error log data:

02:02:32,,CRC,OK,CRC 20708, 039.27, 03.318,22.884512,228.845121

02:02:37,RD,ERROR,ERROR, 000.03, 03.318,22.886202,228.862025

When this error occurred, the UART communications stopped and the test rig power cycled the board 35 seconds later, as designed. When the processor restarted, it completed a full test sequence, but the CRC result was not reported. On subsequent test sequences, the CRC reported “error” because the Flash CRC value being read from the SD card, to compare to the test result, was ‘0’ for the remainder of the test. The team concluded this to be because the SD card build value had been reinitialised after failing to be read, and thus held an correct value. The team did not consider this to be significant because there is no plan to use SD cards in orbit and it is clear from other log data that the processors interface to the SD card is functioning correctly.

6.2.4.2 On-Chip Flash Program Memory

During the destruction test (board 4), at 47 kRads intermittent exception errors began to be reported, when running the Flash memory CRC integrity test. As the TID level increased, the frequency of these errors increased. At 50 kRads the CRC test failed nearly 100% of the time for the remainder of the test, though there were occasions where the test succeeded. The target presented the following exception data to the test rig:

02:14:38,,EXCEPTION,EXCEPTION,R0: b2|R1: 2407fd38|R2: 2407fd48|R3: 8002277|R12: 0|LR: 0|PC: 2407fd58|PSR: 80010e1|BFAR: 8185080|CFSR: 8200|HFSR: 40000000|DFSR: 0|AFSR: 0|

After analysing the exception data output stream, it was determined the error was caused by a corruption of the program memory that caused a jump instruction to have the incorrect destination address. This resulted in the program jumping to a blank area of flash memory, causing a crash and the exception failure. The exceptions appeared to be caused at the same or very similar point in the program code on each test sequence. Unfortunately, because the error was an exception failure, the rest of the test sequence was not completed each time the error was triggered, as a power cycle was required to recover. This resulted in a lack of tests of the FPU and SD-CARD on top of the failing CRC.

6.2.4.3 Reboot Failure

At 97 kRads the processor began to intermittently fail to reset properly after a power cycle. This can be observed in the test file where the timestamps between the exception report and the following reboot, seen where the processor sends

'TIMRQ' to the test rig, are larger than the expected 35-40 seconds. In the lines below, pulled from the test file, the gap between the exception and the following successful reset is 10 minutes. This was in excess of 12 attempted power cycles before a successful reset. This was a strong indicator of further damage to the program memory, suspected to be in the initialisation code.

09:45:25,,EXCEPTION,EXCEPTION,R0: b2|R1: 2407fd38|R2: 2407fd48|R3: 8002277|R12: 0|LR: 0|PC: 2407fd58|PSR: 80010e1|BFAR: 8100000|CFSR: 8200|HFSR: 40000000|DFSR: 0|AFSR: 0|

09:55:04,,TIMRQ,,, 114.01, 11.520,99.613813,996.138128

6.2.5 Annealing Results

A series of annealing tests were conducted after the completion of the destruction test on board 4, which totalled 100 kRads TID, at 1 hour, 5 hours and 3 days following the REEF tests. This differed from the test plan due to access hours available for the REEF lab. The annealing tests conducted at 1 hour and 5 hours showed no improvement on the performance at the end of the destruction test.

The test at 3 days following board 4 destruction test clearly showed annealing improvements in performance. The rebooting failures detailed above were no longer present and the processor successfully rebooted on every power cycle. In addition, the Flash memory CRC test did complete successfully on a number of occasions, and did not constantly throw an exception failure. In addition to this, the current consumption reduced from the value at the end of the destruction test, down from 46 mA to 42 mA. Note: the destruction test began at 38 mA, so this was a 50% reduction of the overall current increase during the test.

6.2.6 Current Consumption Observations

6.2.6.1 10 kRad Mission Duration

As detailed above, the current consumption increase when testing up to 10 kRads was minimal, increasing by 0.7 mA from 39.4 mA to just under 40.1 mA. Figure 12 shows the current profile of the USART tests running on this board, with both the raw measurements taken from the DMM and a rolling average. The raw measurements values are noisy, as expected, as the exact current used during each test can vary with a variety of uncontrollable factors, such as temperature inside the REEF chamber. However, the average line, in red, shows the overall trend in current consumption.

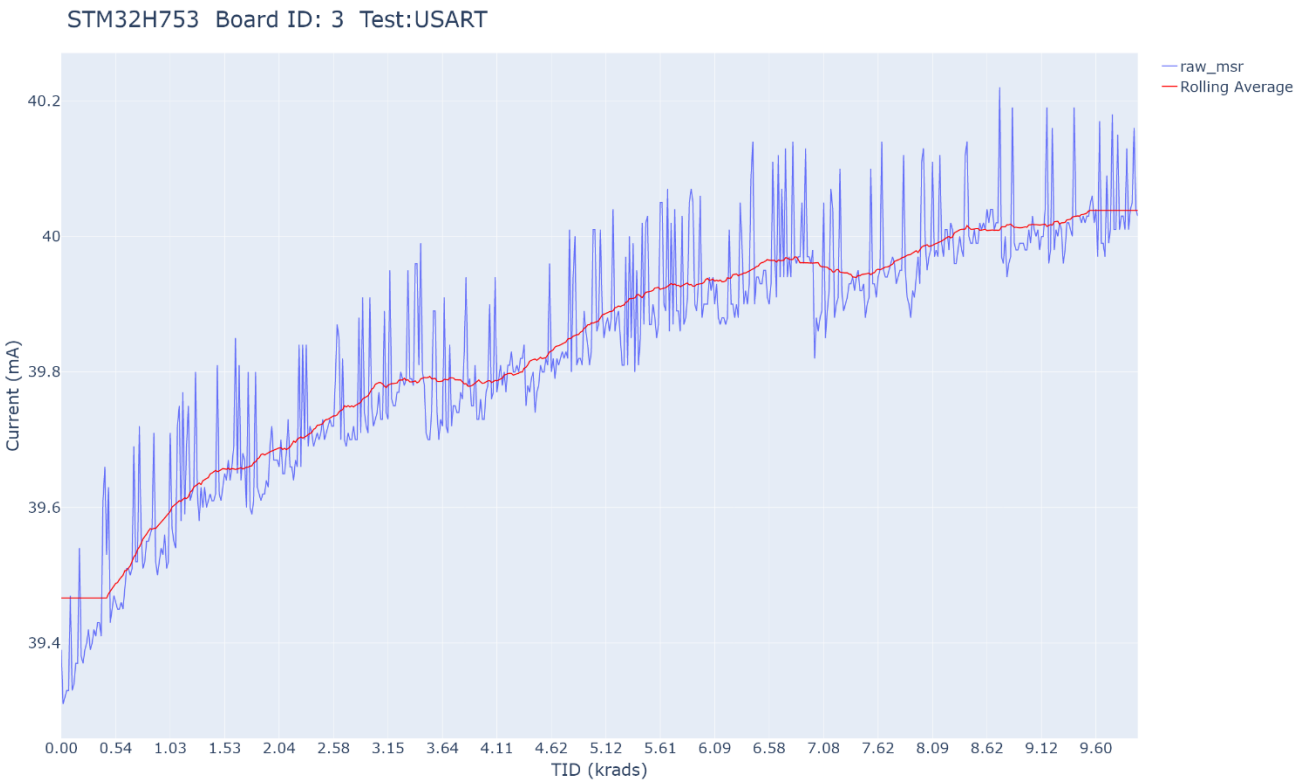

Figure 12: STM32 current consumption for the USART test on Board 3. This board was irradiated until mission specified test value of 10 kRads.

Figure 13: Current consumption of all tests conducted on STM32H753 board 3, up to a TID of 10 krads.

6.2.6.2 Destruction Test

During the destruction test the current continued to increase slowly in roughly linear trend as the TID increased (as seen in Figure 14 for the USART test), until around 45-50 kRads when the rate of increase became greater. This continued at an exponentially increasing rate until the test was stopped. The 45-50 kRads change coincides with beginning of the failures in the flash memory at 47 kRads, and it is likely that this may not be a coincidence as the performance of the processor declined.

Figure 15 shows the current consumption of all the different tests conducted on the STM32H753 during the destruction test. Initially the SD-CARD test draws the most current, along with the UART and USART tests, and the FPU draws the least. At the 47 kRad point, where the CRC failures begin to occur, the current consumption begins to increase exponentially. By the time the test was stopped at 96 kRads, the current had increased to 46.6 mA.

At 78 kRads, the exception failures of the CRC became permanent, resulting in the processor being unable to complete each test loop iteration. This can be seen in Figure 15 where the current lines for the CRC, FPU and SD_CARD tests stop.

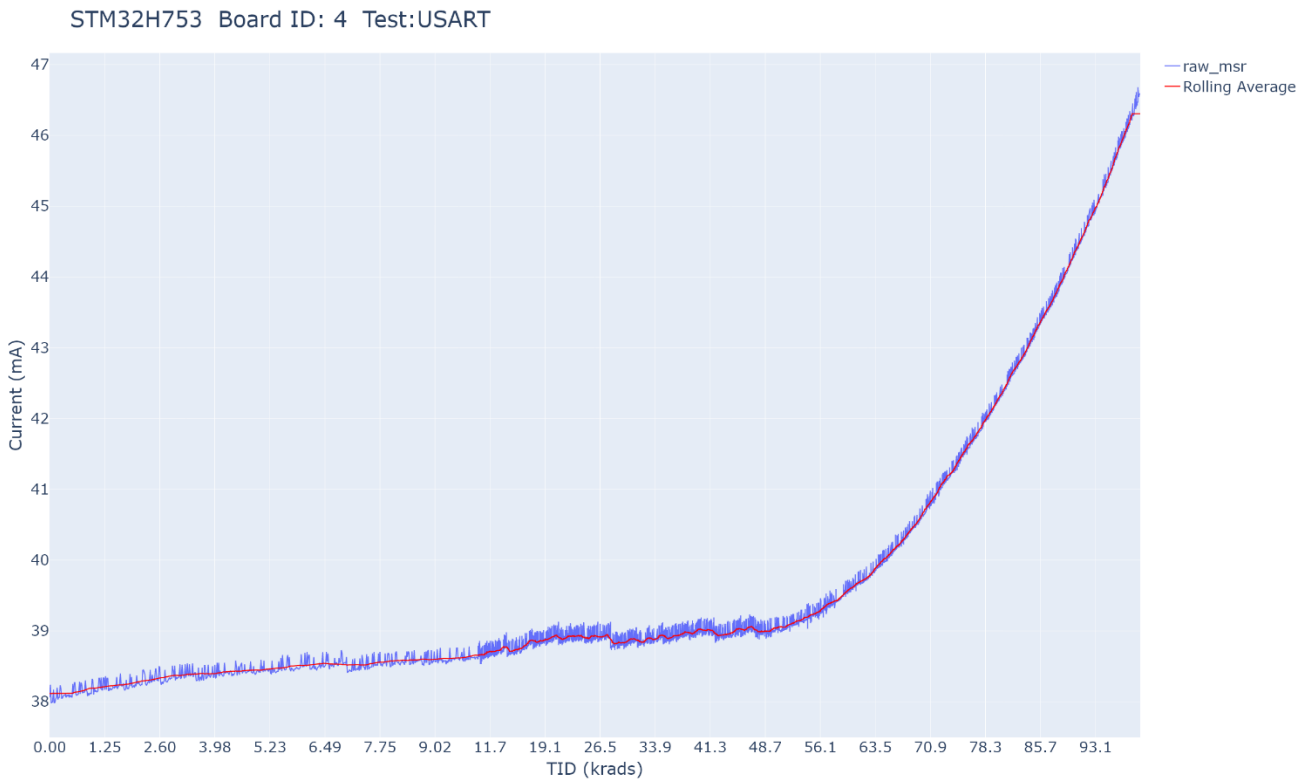

Figure 14: STM32 destruction test, current consumption for the USART test

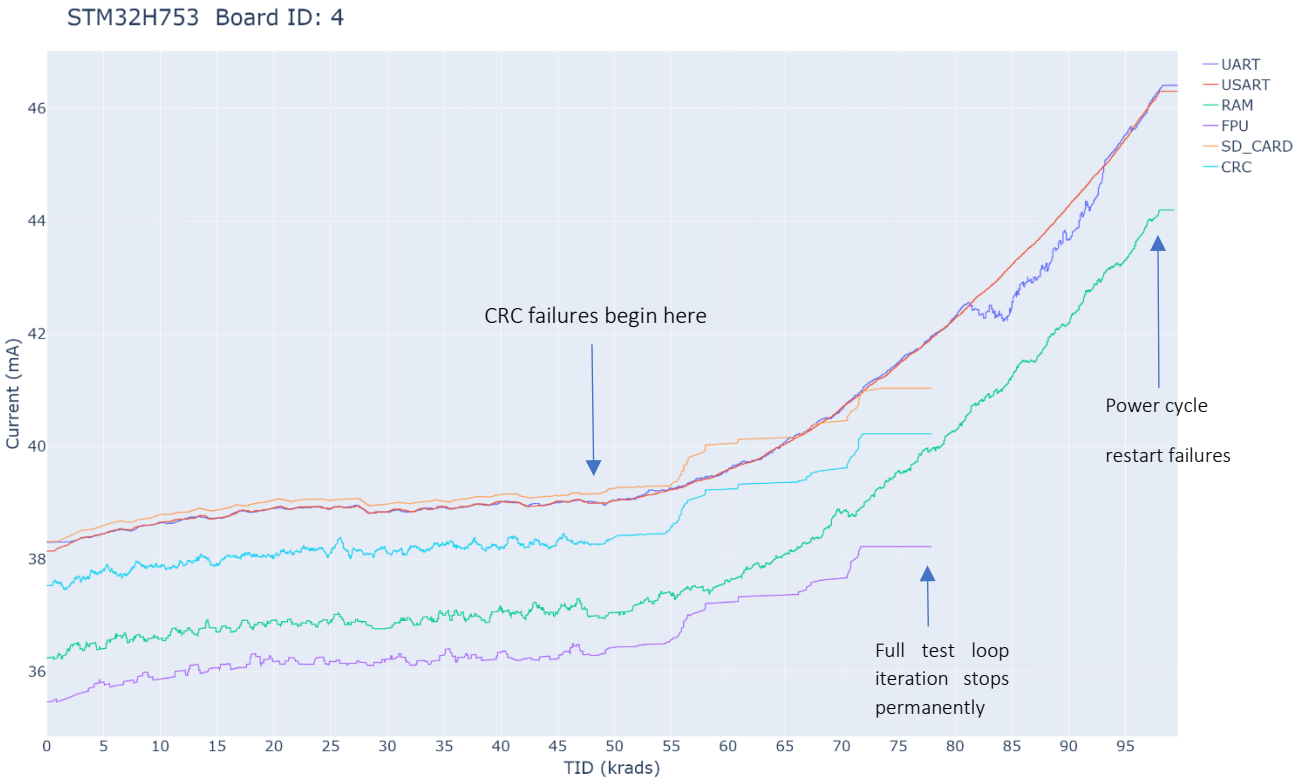

Figure 15: STM32 destruction test, current consumption for the all the tests conducted. The current begins to increase for all tests more rapidly when the CRC/flash memory failures begin to occur. The exceptions on the Flash integrity CRC test occur permanently at 78 kRads, meaning no further tests of the FPU or SD-CARD were conducted either.

6.3 Processor Performance

6.3.1 Test Setup

The OSSAT team is aware that major performance issues occur in relation to writes to a file system. Therefore, in order to assess performance, software was integrated as shown in Figure 16.

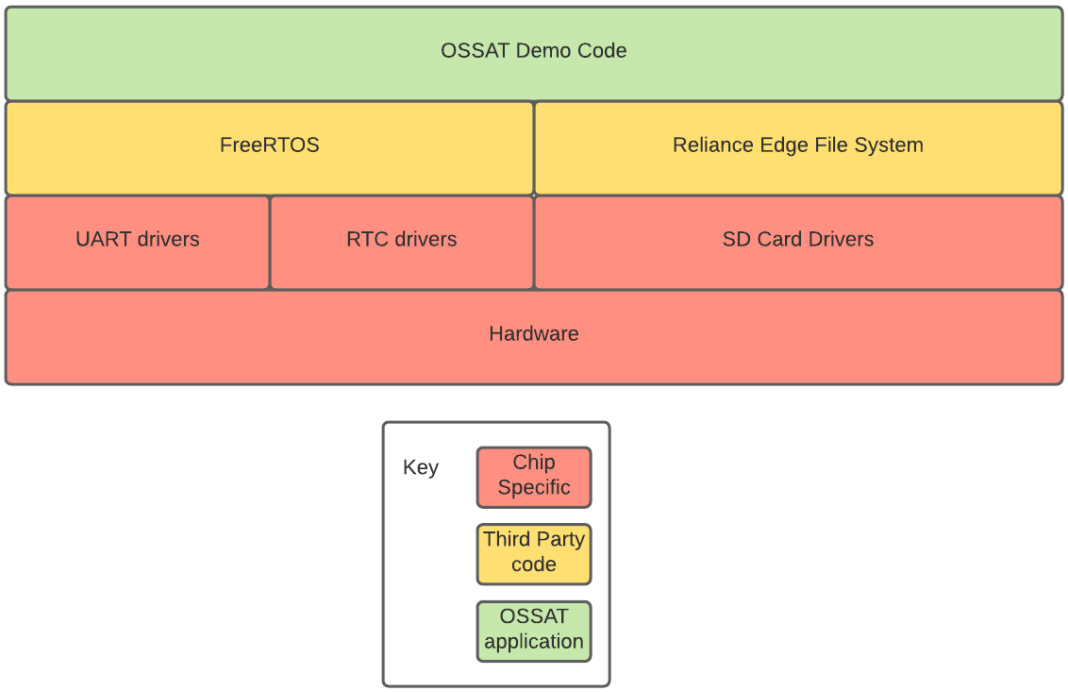

Figure 16: OSSAT SAMV71 file system performance

FreeRTOS was selected because of its strong, open source community, small memory footprint and general simplicity.

The Reliance Edge File System was selected because it is open source and is designed to work reliably following sudden power loss during a commit.

A worst case scenario for platform software file writes was estimated. This resulted in a worst case burst requirement of 6800 bytes across 12 different files in 50ms.

Tests were performed with and without the processor's cache enabled. The feature size of cache means that it is often the weakest part of the chip with respect to single event upset and is therefore often disabled. The STM32H7 has some ECC protection of its cache and therefore, there was interest in understanding the effect of enabling and disabling the cache memory.

6.3.2 Test Results

Tests were run 10 times, writing data to 12 files from 12 different FreeRTOS tasks. This involved the file write and a "red_transact()". This "red_transact()" commits the change to the underlying media (an SD card was chosen). Therefore, the burst requirement of 50ms applies to the file write time only. See section 7 for conclusions.

6.3.2.1 Release build with cache disabled

File write max time: 22.75ms

File write average time: 19.51ms

File write std dev: 2.4ms

red_transact() max time: 63.97ms

6.3.2.2 Release build with cache enabled

File write max time: 20.48ms

File write average time: 17.76ms

File write std dev: 2ms

red_transact() max time: 61.73ms

7 Conclusions

Following the initial testing performed on the STM32H7, it remains a candidate OSSAT processor, both from a performance and radiation tolerance perspective. Further work is needed to validate this further.

It is capable of writing to files at a speed which is fast enough for the needs of the OSSAT platform requirements (with cache enabled consuming approximately. 40% of the processor's processing run time under worst case burst write conditions).

It is also capable of withstanding significant TID without failure. Through analysis, a 10 year 800km sun synchronous orbit would equate to approximately 10 kRads of radiation dose. Under the destruction test, the chip only began to fail at 47 kRads. The current increase observed was reasonably significant but not until the 47kRads failures were observed. An overall increase of 9mA (a 24% increase) was observed at 100 kRads. It should also be noted that annealing had a big impact on the processor's performance; this is another positive sign that the processor is capable of withstanding the radiation dose.

8 Future Work

Further work is required in order to derisk the STM32H7 as a suitable processor for the OSSAT platform. The OSSAT team are therefore planning the following:

8.1 SEU/Latch-up testing

The OSSAT team have a test plan drafted for a proton irradiation test campaign to test for tolerance against the Single Event Upset and Latch up effects.

8.2 Further performance testing

The design goal is to develop an AOCS system capable of running AOCS loops at up to 12Hz. This would be a major performance requirement on the STM32H7 processor. Therefore, a further task would be to develop representative AOCS software that would exercise the processor and assess its suitability to this task.

9 Credits

Many thanks to Research England and SPRINT for supporting this project, to the University of Surrey for their contribution and to the growing and amazing collaborators who make up the OSSAT team. This includes Dr Keith Ryden, Dr Benjamin Clewer, Dr Alex Hands, Jamie Bayley, Dr Chris Bridges, Dr John Paffett, Paul Madle, Anita Bernie, Angela Brown, Mauricio De Carvalho and Ian James.

10 Appendix A

The ARM Cortex M7 core incorporates ECC protection on its instruction and data cache that recovers from errors. The following table shows how different types of cache RAM are protected:

RAM type	Protection	Recoverable error	Non-recoverable error	Hard error support
Data tag RAM	SEC-DED ECC	Error seen as single bit errors	Error seen as a multiple bit error	Up to two hard errors
Data cache data RAM	SEC-DED ECC	Error seen as single bit errors	Error seen as a multiple bit error on dirty lines	
Instruction tag RAM	SEC-DED ECC	Any error, single or double, on the tag or valid bit stored in the RAM	None[a]	
Instruction cache data RAM	SEC-DED ECC	Any error on the data stored in the RAM	None[a]	

a. The instruction cache is never dirty so cache RAM errors are always recoverable by invalidating the cache and retrying the instruction.

Figure 17: Cortex M7 ECC features

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